IT IS CLAIMED:

1. A method of making an array of non-volatile memory cells on a semiconductor substrate surface, comprising:

forming an array of first floating gate portions across the substrate surface with a gate dielectric layer therebetween,

forming a masking layer over areas of the substrate not covered by first floating gate portions such that a pattern of openings in the masking layer is self-aligned to the first floating gate portions,

forming sidewall elements in the openings in the masking layer over first floating gate portions,

forming second floating gate portions defined by the sidewall elements in at least one direction and contacting the first floating gate portion.

2. The method of claim 1, wherein the first floating gate portions are formed by depositing a layer of gate material, thereafter depositing a layer of dielectric material over the gate material, thereafter etching the dielectric material and gate material in the same pattern to form structures comprising first floating gate portions covered by dielectric material.

3. The method of claim 2 further comprising implanting impurities into the substrate while first floating gate portions covered by dielectric material are present so as to implant impurities only in the areas of the substrate not covered by floating gate portions covered by dielectric material.

4. The method of claim 2, wherein the masking layer is formed by depositing masking layer material over the surface of the substrate and thereafter removing masking layer material that overlies first floating gate portions covered by dielectric material.

5. The method of claim 4, wherein the dielectric material is removed after the masking layer material that overlies first floating gate portions covered by dielectric material is removed.

6. The method of claim 1, wherein the sidewall portions are formed by deposition and etch back of silicon nitride.

7. The method of claim 1, wherein the second floating gate portion is formed by deposition and etch back of polysilicon.

8. The method of claim 1, further comprising:
removing the sidewall elements thereby exposing surfaces of the first and second floating gate portions,
forming a dielectric layer on the exposed floating gate portion surfaces, and
forming conductive gates extending across the floating gates in at least one direction and in contact with the dielectric layer.

9. The method of claim 8, wherein the dielectric layer is an ONO layer.

10. The method of claim 8, wherein the conductive gates extend towards the surface of the semiconductor substrate such that the lowest extremities of the conductive gates are closer to the surface of the semiconductor substrate than the highest extremities of the second floating gate portions.

11. The method of claim 10 wherein the conductive gates extend to enclose the second floating gate portions from above and on four lateral sides.

12. The method of claim 8 further comprising the step of depositing a metal on the conductive polysilicon gates and exposing to increased temperature to produce a silicide layer.

13. A non-volatile memory cell array of conductive floating gates arranged in strings across a surface of a substrate, each string comprising floating gates aligned along the string and separated from adjacent strings by isolating elements, wherein the floating gates individually comprise a first floating gate portion that has an upper surface and a lower surface both upper and lower surfaces being parallel to the surface of the substrate and a second floating gate portion that extends from a first region of the upper surface of the first floating gate portion and wherein the first region is between a second region and a third region of the upper surface of the first floating gate portion along the direction of the string.

14. The memory cell array of claim 13, wherein each second floating gate portion extends from the upper surface of the first floating gate portion to form an inverted T shape in cross-section.

15. The memory cell array of claim 13, wherein the second floating gate portion extends at least to the edges of the upper surface of the first floating gate portion in a direction perpendicular to the direction of the string and the second floating gate portion does not extend to the edges of the upper surface of the first floating gate portion along the direction of the string.

16. The memory cell array of claim 13 wherein the second floating gate portion extends from one isolating element to an adjacent isolating element at the upper surface of the first floating gate portion and extents over the first isolating element and the second isolating element at a level above the surface of the first floating gate.

17. A floating gate in a string of floating gates, the floating gate comprising a first floating gate portion that extends across the surface of a substrate and a second floating gate portion that extends along a plane that is perpendicular to the surface of the substrate and wherein the plane of the second floating gate portion bisects the first

floating gate portion and wherein the plane of the second floating gate portion is perpendicular to the string

18. A method of making an array of non-volatile memory cells on a semiconductor substrate surface, comprising:
forming an array of first floating gate portions, wherein each first floating gate portion is physically separated from adjacent first floating gate portions,
thereafter forming second floating gate portions extending from first floating gate portions, wherein each second floating gate portion extends along a plane perpendicular to the plane of the substrate surface and wherein the plane of the second floating gate portion bisects the first floating gate portion.

19. The method of claim 18 wherein the first floating gate portions are square in shape and the second portions extend from a line that is approximately a midline of the square.